



# MIC2564A

## Dual Serial PCMCIA/CardBus Power Controller

### General Description

The MIC2564A is dual-slot PC Card PCMCIA (Personal Computer Memory Card International Association) and CardBus power controller. It is a sophisticated power switching matrix that controls  $V_{CC}$  and  $V_{PP}$  voltages to two PC Card slots. The MIC2564A is used in conjunction with a serial-data output logic controller using the standard three-wire serial control data format.

When connected to 3.3V, 5V, and 12V system power supplies, the MIC2564A can switch its  $V_{CC}$  outputs between 0V, 3.3V, 5.0V, and high-impedance states and  $V_{PP}$  outputs between 0V, 3.3V, 5V, 12V, and high-impedance states. The  $V_{CC}$  outputs will supply a minimum of 1A current to the socket and the  $V_{PP}$  outputs will supply a minimum of 120mA to the socket. Voltage rise and fall times are well controlled. The MIC2564A also features an efficient standby (sleep) mode at 0.3 $\mu$ A typical quiescent current.

12V and 5V supplies are not required for MIC2564A operation making it possible to omit one or both supplies when they are not needed by the system. An internal charge pump supplies the internal bias voltages required for high-performance switching.

The MIC2564A is protected by overtemperature shutdown, and protects itself and the system with current limiting and cross-conduction lockout.

The MIC2564A is available in 24-pin SSOP, 24-pin TSSOP, and an environmentally friendly (lead-free) 24-pin TSSOP.

All support documentation can be found on Micrel's web site at [www.micrel.com](http://www.micrel.com).

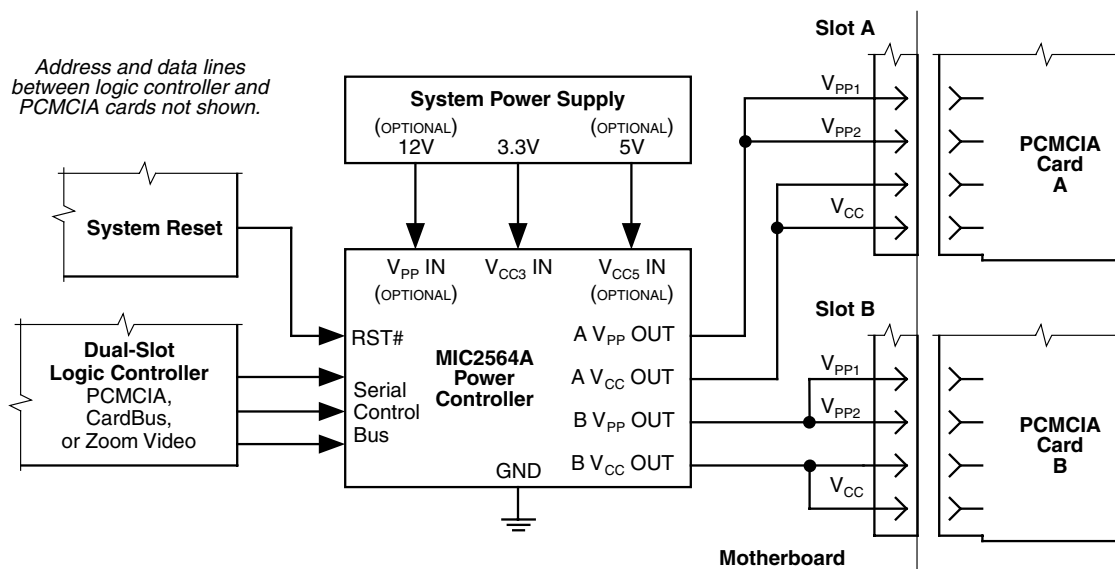
### Features

- Standard 3-wire serial control data input
- Controls two card slots from one surface mount device
- High-efficiency, low-resistance switches
- 12V supply optional (not required by MIC2564A)
- Current limit and overtemperature shutdown
- Ultra-low 1 $\mu$ A-typical standby power consumption
- Cross-conduction lockout (no switching transients)
- Break-before-make switching
- 1A minimum  $V_{CC}$  output per slot
- Independent  $V_{CC}$  and  $V_{PP}$  voltage output (MIC2564A-1)
- 120mA minimum  $V_{PP}$  output current per slot
- Lead-free 24-pin surface-mount TSSOP package
- UL recognized, file #179633

### Applications

- PC Card and CardBus power control
- Zoom Video port power control
- Wireless communications
- Bar code data collection systems
- Docking stations (portable and desktop)
- Power supply management

### Typical Application



UL Recognized Component

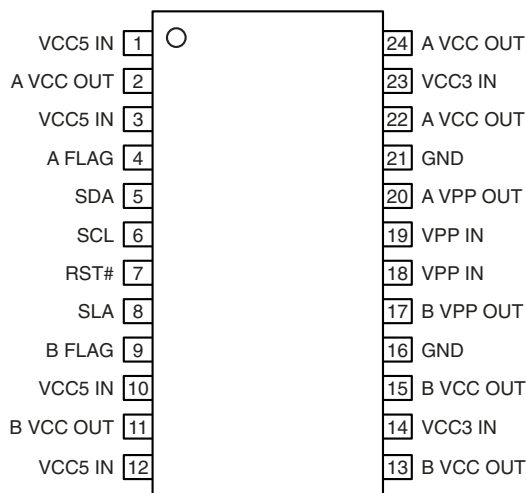
### PCMCIA Card Power Management Application

## Ordering Information

Part Number	Temperature Range	Package	Lead-Finish
MIC2564A-0BSM	-40°C to +85°C	24-pin SSOP	Standard
MIC2564A-1BSM*	-40°C to +85°C	24-pin SSOP	Standard
MIC2564A-0BTS	-40°C to +85°C	24-pin TSSOP	Standard
MIC2564A-1BTS*	-40°C to +85°C	24-pin TSSOP	Standard
MIC2564A-0YTS	-40°C to +85°C	24-pin TSSOP	Lead-free
MIC2564A-1YTS*	-40°C to +85°C	24-pin TSSOP	Lead-free

\* -1 option: independent V<sub>PP</sub> OUT and V<sub>CC</sub> OUT programming

## Pin Configuration



**24-lead SSOP (SM)**

**24-lead TSSOP (TS)**

## Pin Description

Pin Number	Pin Name	Pin Function
1, 3, 10, 12	VCC5 IN	5V Supply Input: Optional system power supply connection. Required only for 5V V <sub>CC</sub> and V <sub>PP</sub> output voltage.
2, 22, 24	A VCC OUT	Slot A V <sub>CC</sub> Output: Pins 2, 22 and 24 must be externally connected together.
4	A FLAG	Channel A V <sub>CC</sub> and V <sub>PP</sub> Output Monitor (Output): Low on error condition.
5	SDA	Serial Data (Input).
6	SCL	Serial Clock (Input).
7	RST#	System Reset (Input): Active low signal deactivates the MIC2564A, clearing the serial registers and forcing the four power outputs to 0V (GND).
8	SLA	Serial Data Latch (Input).
9	B FLAG	Channel B V <sub>CC</sub> and V <sub>PP</sub> Output Monitor (Output): Low on error condition.
11, 13, 15	B VCC OUT	Slot B V <sub>CC</sub> Output: Pins 11, 13 and 15 must be externally connected together.
14, 23	VCC3 IN	3.3V Supply Input: Required system power supply connection. Powers 3.3V V <sub>CC</sub> and V <sub>PP</sub> outputs and all internal circuitry.
16, 21	GND	Ground.
17	B VPP OUT	Slot B V <sub>PP</sub> Output.
18, 19	VPP IN	12V Supply Input: Optional system power supply connection. Required only for 12V V <sub>PP</sub> output voltage.
20	A VPP OUT	Slot A V <sub>PP</sub> Output.

**Absolute Maximum Ratings<sup>(1)</sup>**

V <sub>PP</sub> IN	+13.6V
V <sub>CC3</sub> IN	+6.0V
V <sub>CC5</sub> IN	+6.0V
V <sub>SCL</sub> , V <sub>SDA</sub> , V <sub>SLA</sub> , V <sub>RST#</sub>	-0.3V to +6.0V
V <sub>A</sub> FLAG, V <sub>B</sub> FLAG	+6.0V
A or B V <sub>PP</sub> OUT	>120mA, Internally Limited
A or B V <sub>CC</sub> OUT	>1A, Internally Limited
Power Dissipation (P <sub>D</sub> ) at T <sub>A</sub> ≤ 25°C	Internally Limited
Storage Temperature	-65°C to +150°C
Lead Temperature (5 sec.)	+260°C
ESD Rating <sup>(3)</sup>	

**Operating Ratings<sup>(2)</sup>**

V <sub>PP</sub> IN	0V to +13.2V
V <sub>CC3</sub> IN	+3.0V to +5.5V
V <sub>CC5</sub> IN	0V to +5.5V
V <sub>SCL</sub> , V <sub>SDA</sub> , V <sub>SLA</sub> , V <sub>RST#</sub>	0V to +5.5V
A or B V <sub>PP</sub> OUT	0 to 120mA
A or B V <sub>CC</sub> OUT	0 to 1A
Clock Frequency	0 to 2MHz
Ambient Temperature (T <sub>A</sub> )	-40°C to +85°C
Junction Temperature (T <sub>J</sub> )	+125°C
Package Thermal Resistance	
SSOP (θ <sub>JA</sub> )	90°C/W
TSSOP (θ <sub>JA</sub> )	83°C/W

**Electrical Characteristics<sup>(4)</sup>**

V<sub>CC3</sub> IN = 3.3V, V<sub>CC5</sub> IN = 5.0V, V<sub>PP</sub> IN = 12V; T<sub>A</sub> = 25°C, **bold** indicates -40°C ≤ T<sub>A</sub> ≤ +85°C; unless noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>V<sub>PP</sub> Output</b>						
I <sub>PP</sub> OUT Hi-Z	High-Impedance Output Leakage Current	Shutdown mode V <sub>PP</sub> OUT = 0V		1	10	μA
I <sub>PPSC</sub>	Short Circuit Current Limit	V <sub>PP</sub> OUT = 0V, normal mode <sup>(5)</sup>	120	260	400	mA
R <sub>O</sub>	Switch Resistance	V <sub>PP</sub> OUT = 5V selected, I <sub>PP</sub> OUT = -100mA (sourcing)		1.6	<b>5</b>	Ω
		V <sub>PP</sub> OUT = 3.3V selected, I <sub>PP</sub> OUT = -100mA (sourcing)		1.3	<b>5</b>	Ω
		V <sub>PP</sub> OUT = 12V selected, V <sub>PP</sub> IN = 12V, I <sub>PP</sub> OUT = -100 mA (sourcing)		1.3	<b>2.3</b>	Ω
		V <sub>PP</sub> OUT = 0V [ground] selected, I <sub>PP</sub> OUT = 50μA (sinking)		2000	<b>5000</b>	Ω
<b>V<sub>PP</sub> Switching Time</b> (See Figure 3)						
t <sub>1</sub>	Output Turn-On Delay <sup>(6)</sup>	V <sub>PP</sub> OUT = Hi-Z to 10% of 3.3V, R <sub>L</sub> = 100Ω		1	100	μs
t <sub>2</sub>		V <sub>PP</sub> OUT = Hi-Z to 10% of 5V, R <sub>L</sub> = 100Ω		1	100	μs
t <sub>3</sub>		V <sub>PP</sub> OUT = Hi-Z to 10% of 12, R <sub>L</sub> = 100Ω		50	250	μs
t <sub>4</sub>	Output Rise Time	V <sub>PP</sub> OUT = 10% to 90% of 3.3, R <sub>L</sub> = 100Ω	10	100	500	μs
t <sub>5</sub>		V <sub>PP</sub> OUT = 10% to 90% of 5, R <sub>L</sub> = 100Ω	10	250	1000	μs
t <sub>6</sub>		V <sub>PP</sub> OUT = 10% to 90% of 12, R <sub>L</sub> = 100Ω	10	100	500	μs
t <sub>7</sub>	Output Transition Time <sup>(6)</sup>	V <sub>PP</sub> OUT = 3.3V to 90% of 12V, R <sub>L</sub> = 100Ω	10	100	500	μs
t <sub>8</sub>		V <sub>PP</sub> OUT = 5V to 90% of 12, R <sub>L</sub> = 100Ω	10	100	500	μs
t <sub>9</sub>		V <sub>PP</sub> OUT = 12V to 90% of 3.3, R <sub>L</sub> = 100Ω	10	100	500	μs
t <sub>10</sub>		V <sub>PP</sub> OUT = 12V to 90% of 5, R <sub>L</sub> = 100Ω	10	250	1000	μs
t <sub>11</sub>	Output Turn-Off Fall Time	V <sub>PP</sub> OUT = 90% to 10% of 3.3, R <sub>L</sub> = 100Ω		1	500	μs
t <sub>12</sub>		V <sub>PP</sub> OUT = 90% to 10% of 5, R <sub>L</sub> = 100Ω		1	500	μs
t <sub>13</sub>		V <sub>PP</sub> OUT = 90% to 10% of 12, R <sub>L</sub> = 100Ω		1	500	μs

**Notes:**

- Exceeding the absolute maximum rating may damage the device.
- The device is not guaranteed to function outside its operating rating.
- Devices are ESD sensitive. Handling precautions recommended.
- Specification for packaged product only.
- Output enabled into short circuit.
- Measurement is from the 50% point of the SLA rising edge.

## Electrical Characteristics<sup>(7)</sup>

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t <sub>14</sub>	Output Turn-Off Delay Time <sup>(8, 11)</sup>	V <sub>PP</sub> OUT = 3.3V to Hi-Z, R <sub>L</sub> = 100Ω		1	50	μs
t <sub>15</sub>		V <sub>PP</sub> OUT = 5V to Hi-Z, R <sub>L</sub> = 100Ω		1	50	μs
t <sub>16</sub>		V <sub>PP</sub> OUT = 12V to Hi-Z, R <sub>L</sub> = 100Ω		1	50	μs

### V<sub>CC</sub> Output

I <sub>CC</sub> OUT Hi-Z	High-Impedance Output Leakage Current	Shutdown mode, V <sub>CC</sub> OUT = 0V		1	20	μA
I <sub>CCSC</sub>	Short Circuit Current Limit	V <sub>CC</sub> OUT = 0, normal mode, V <sub>CC3</sub> or V <sub>CC5</sub> switches <sup>(9)</sup>	1.0	2.0	3.0	A
R <sub>O</sub>	Switch Resistance	V <sub>CC</sub> OUT = 3.3V selected, I <sub>CC</sub> OUT = -1A (sourcing)		120	<b>150</b>	mΩ
		V <sub>CC</sub> OUT = 5V selected, I <sub>CC</sub> OUT = -1A (sourcing)		85	<b>120</b>	mΩ
		V <sub>CC</sub> OUT = 0V [ground] selected, I <sub>CC</sub> OUT = 0.1mA (sinking)		2000	<b>3900</b>	Ω

### V<sub>CC</sub> Switching Time (See Figure 4)

t <sub>17</sub>	Output Turn-On Delay Time <sup>(8)</sup>	V <sub>CC</sub> OUT = 0V to 10% of 3.3, R <sub>L</sub> = 10Ω		250	500	μs
t <sub>18</sub>		V <sub>CC</sub> OUT = 0V to 10% of 5.0, R <sub>L</sub> = 10Ω		500	1000	μs
t <sub>19</sub>	Output Rise Time	V <sub>CC</sub> OUT = 10% to 90% of 3.3V, R <sub>L</sub> = 10Ω	750	1200	5000	μs
t <sub>20</sub>		V <sub>CC</sub> OUT = 10% to 90% of 5, R <sub>L</sub> = 10Ω	1000	2200	5000	μs
t <sub>21</sub>	Output Fall Time	V <sub>CC</sub> OUT = 90% to 10% of 3.3, R <sub>L</sub> = 10Ω	100	550	1000	μs
t <sub>22</sub>		V <sub>CC</sub> OUT = 90% to 10% of 5.0, R <sub>L</sub> = 10Ω	100	400	2000	μs
t <sub>23</sub>	Output Turn-Off Delay <sup>(8, 10)</sup>	V <sub>CC</sub> OUT = 3.3V to 90% of 3.3V, R <sub>L</sub> = 10Ω		400	2000	μs
t <sub>24</sub>		V <sub>CC</sub> OUT = 5V to 90% of 5V, R <sub>L</sub> = 10Ω		400	2000	μs

### Power Supply

I <sub>CC3</sub>	V <sub>CC3</sub> IN Supply Current (3.3V) <sup>(11)</sup>	V <sub>CC</sub> OUT = 5V or 3.3V, I <sub>CC</sub> OUT = 0		120	200	μA
		V <sub>CC</sub> OUT = Hi-Z (sleep mode)		5	10	μA
I <sub>CC5</sub>	V <sub>CC5</sub> IN Supply Current (5V) <sup>(12)</sup>	V <sub>CC</sub> OUT = 5V or 3.3V, I <sub>CC</sub> OUT = 0		25	50	μA
		V <sub>CC</sub> OUT = Hi-Z (sleep mode)		0.2	10	μA
I <sub>PP</sub> IN	V <sub>PP</sub> IN Supply Current (12V) <sup>(12)</sup>	V <sub>PP</sub> OUT = 0V, 3.3V, 5V, or Hi-Z; I <sub>PP</sub> OUT = 0		1	10	μA
		V <sub>PP</sub> OUT = V <sub>PP</sub> IN		4	50	μA
V <sub>CC3</sub>	Operating Input Voltage (3.3V)	<b>Note 11</b>	3.0	3.3	5.5	V
V <sub>CC5</sub>	Operating Input Voltage (5V)	<b>Note 12</b>		5.0	5.5	V
V <sub>PP</sub>	Operating Input Voltage (12V)	<b>Notes 12, 13</b>		12	13.2	V

#### Notes:

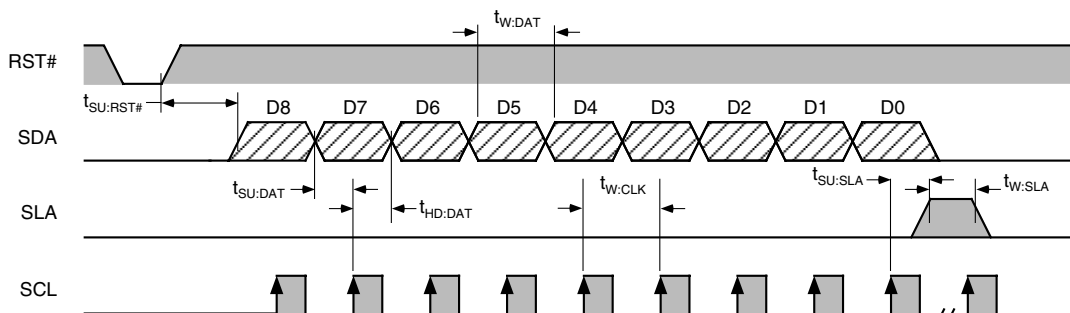
7. Specification for packaged product only.
8. Measurement is from the 50% point of the SLA rising edge.
9. Output enabled into short circuit.
10. Measurement is from the Hi-Z- or 0V-state command to the beginning of the slope. Measurement does not apply when device is in current limit or thermal shutdown.
11. V<sub>CC3</sub> IN powers all internal logic, bias, and drive circuitry, and is required for operation.
12. V<sub>PP</sub> and V<sub>CC5</sub> IN are not required for operation.
13. V<sub>PP</sub> IN must be either high-impedance or greater than or approximately equal to the highest voltage V<sub>CC</sub> in the system. For example, if both 3.3V and 5V are connected to the MIC2564A, V<sub>PP</sub> IN must be either 5V, 12V, or high-impedance.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>Thermal Shutdown</b>						
$T_{SD}$	Thermal Shutdown Temperature			145		°C
<b>Serial Interface DC Specifications</b>						
$V_{IH}$	Input Voltage: SDA, SCL, SLA pins		$0.7V_{CC3IN}$		5.5	V
$V_{IL}$	Input Voltage: SDA, SCL, SLA pins		-0.3		$0.3V_{CC3IN}$	V
$I_{IN}$	Input Current	$0V < V_{IN} < 5.5V$	-1	0.2	1	μA
<b>Flag</b>						
$I_{FLG}$	Flag Leakage Current	$V_{FLG} = 5V$			1	μA
<b>Serial Interface Timing Requirements (See Figures 1 and 2)<sup>(14)</sup></b>						
$t_{HD:DAT}$	SDA Hold Time		75			ns
$t_{SU:DAT}$	SDA Setup Time	Data before clock	75			ns
$t_{SU:SLA}$	Latch Setup Time		50			ns
$t_{SU:RST\#}$	Reset to Data Setup Time	RST# before data	50			ns
$t_W$	Minimum Pulse Width	Clock ( $t_{W:CLK}$ )	50			ns
		Latch ( $t_{W:SLA}$ )	100			ns
		Reset ( $t_{W:RST}$ )	50			ns
		Data ( $t_{W:DA}$ )	50			ns
$t_R$	SCL Rise Time	$f = 32kHz^{(15)}$	0		100	ns
$t_F$	SCL Fall Time	$f = 32kHz^{(15)}$	0		100	ns

**Notes:**

- 14. Guaranteed by design not production tested.
- 15. Guaranteed by characterization but not production tested.

**Serial Control Timing Diagram**



**Figure 1. Serial Control Timing Diagram**

The MIC2564A uses a three-wire serial interface to control  $V_{CC}$  and  $V_{PP}$  outputs for both sections A and B. The three control lines have thresholds compatible with both 3.3V and 5V logic families. Data (SDA) is clocked in on the rising clock edge. The clock signal may be continuous or it may halt after all data is clocked in.



**Figure 2. SCL Rise and Fall Times**

## Output Timing Diagrams

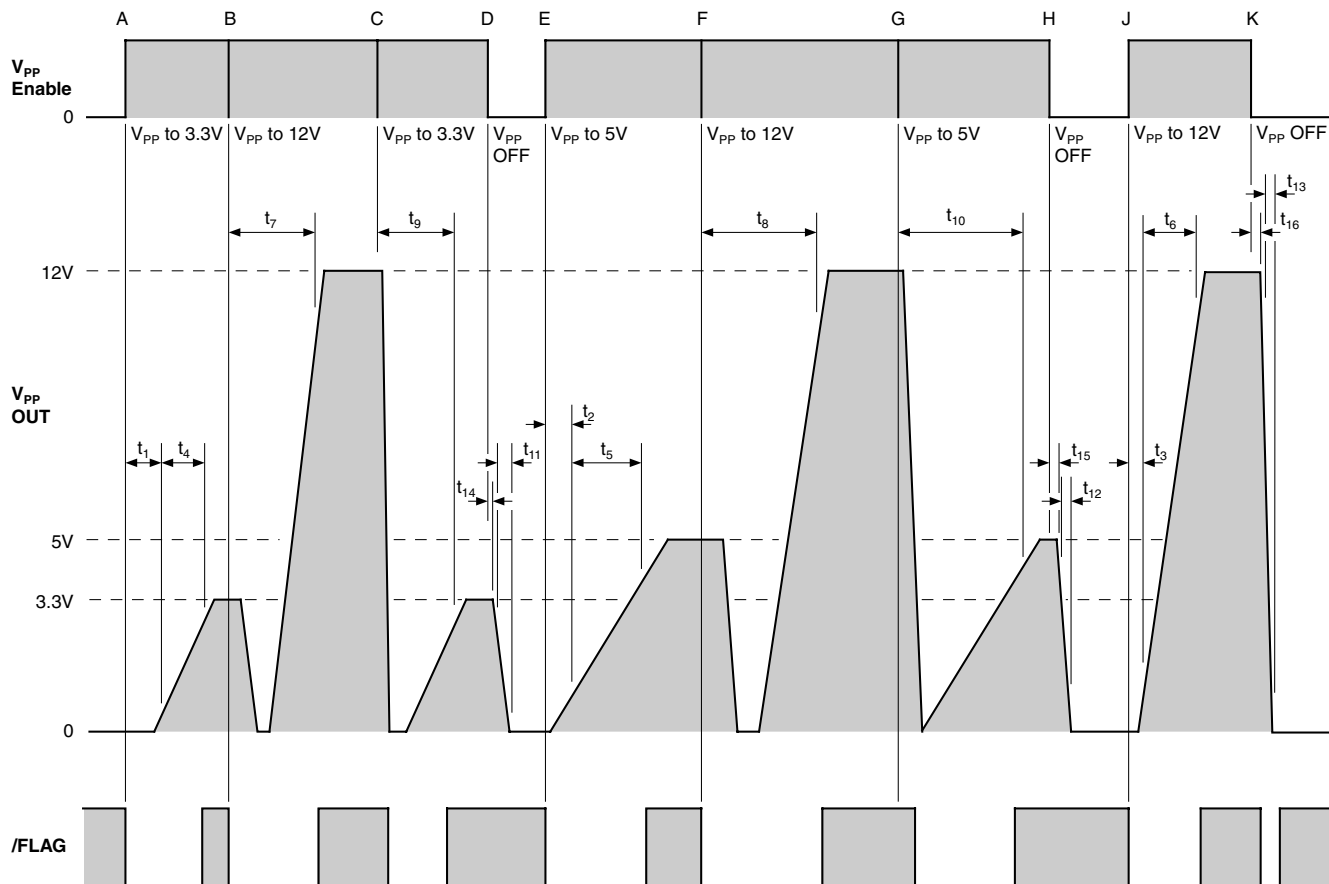


Figure 3. V<sub>PP</sub> Timing Diagram

V<sub>PP</sub> Enable is shown generically. R<sub>L</sub> = 100Ω. C<sub>L</sub> = negligible. Refer to the serial control timing diagrams for details.

At time "A", V<sub>PP</sub> = 3.3V is selected, "B", V<sub>PP</sub> is set to 12V, "C", V<sub>PP</sub> = 3.3V (from 12V), "D", V<sub>PP</sub> is disabled, "E", V<sub>PP</sub> is programmed to 5V, "F", V<sub>PP</sub> is set to 12V, "G", V<sub>PP</sub> is programmed to 5V, "H", V<sub>PP</sub> is disabled, "J", V<sub>PP</sub> is set to 12V, "K", V<sub>PP</sub> is again disabled.

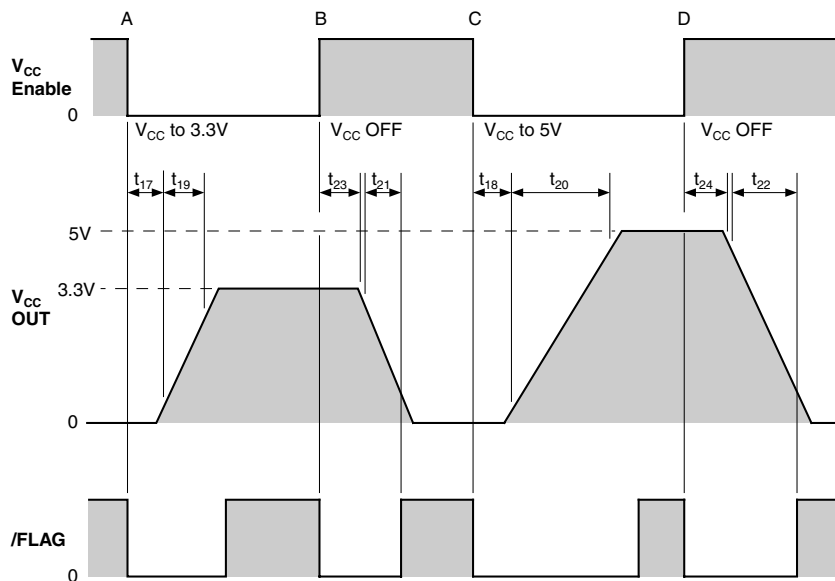


Figure 4. V<sub>CC</sub> Timing Diagram

V<sub>CC</sub> Enable is shown generically. R<sub>L</sub> = 10Ω. Refer to the serial control timing diagrams for specific control logic input.

At time "A", V<sub>CC</sub> is programmed to 3.3V, "B", V<sub>CC</sub> is disabled, "C", V<sub>CC</sub> is programmed to 5V, "D", V<sub>CC</sub> is disabled.

**MIC2564A-0 Logic Table**

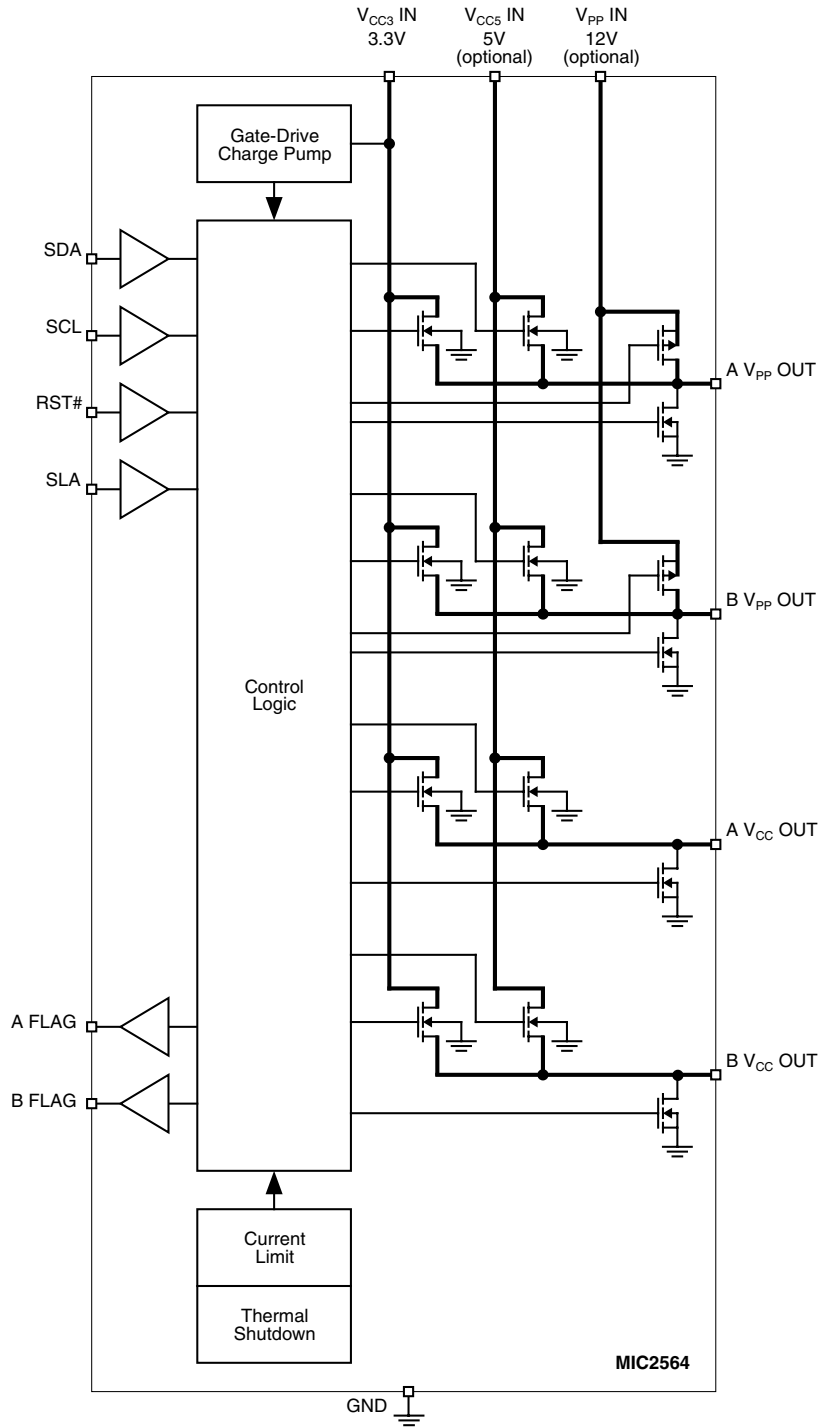
D8	D7	D6	D5	D4	D3	D2	D1	D0	B V <sub>CC5</sub> OUT	B V <sub>CC3</sub> OUT	B V <sub>PP_PGM</sub> OUT	A V <sub>CC5</sub> OUT	A V <sub>CC3</sub> OUT	A V <sub>PP_PGM</sub> OUT	B V <sub>PP</sub> OUT	B V <sub>CC</sub> OUT	A V <sub>PP</sub> OUT	A V <sub>CC</sub> OUT
SHDN	B V <sub>CC5</sub>	B V <sub>CC3</sub>	B V <sub>PP_VCC</sub>	B V <sub>PP_PGM</sub>	A V <sub>CC5</sub>	A V <sub>CC3</sub>	A V <sub>PP_VCC</sub>	A V <sub>PP_PGM</sub>	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
0	X	X	X	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
1									0V*	0V*	0V*	0V*	0V*	0V*	0V*	0V*	0V*	0V*
1					0	0	0	0	12V†	12V†	12V†	12V†	12V†	12V†	12V†	12V†	12V†	12V†
1					0	0	0	1	0V*	0V*	0V*	0V*	0V*	0V*	0V*	0V*	0V*	0V*
1					0	0	1	1	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
1					0	1	0	0	0V*	0V*	0V*	0V*	0V*	0V*	0V*	0V*	0V*	0V*
1					0	1	0	1	12V	12V	12V	12V	12V	12V	12V	12V	12V	12V
1					0	1	1	0	3.3V	3.3V	3.3V	3.3V	3.3V	3.3V	3.3V	3.3V	3.3V	3.3V
1					0	1	1	1	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
1					1	0	0	0	0V*	0V*	0V*	0V*	0V*	0V*	0V*	0V*	0V*	0V*
1					1	0	0	1	12V	12V	12V	12V	12V	12V	12V	12V	12V	12V
1					1	0	1	0	5V	5V	5V	5V	5V	5V	5V	5V	5V	5V
1					1	0	1	1	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
1					1	1	0	0	0V*	0V*	0V*	0V*	0V*	0V*	0V*	0V*	0V*	0V*
1					1	1	0	1	12V†	12V†	12V†	12V†	12V†	12V†	12V†	12V†	12V†	12V†
1					1	1	1	0	0V*	0V*	0V*	0V*	0V*	0V*	0V*	0V*	0V*	0V*
1					1	1	1	1	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
1					0	0	0	0	0V*	0V*	0V*	0V*	0V*	0V*	0V*	0V*	0V*	0V*
1					0	0	0	1	12V†	12V†	12V†	12V†	12V†	12V†	12V†	12V†	12V†	12V†
1					0	0	1	0	0V*	0V*	0V*	0V*	0V*	0V*	0V*	0V*	0V*	0V*
1					0	1	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
1					0	1	0	1	0V*	0V*	0V*	0V*	0V*	0V*	0V*	0V*	0V*	0V*
1					0	1	1	0	12V	12V	12V	12V	12V	12V	12V	12V	12V	12V
1					0	1	1	1	5V	5V	5V	5V	5V	5V	5V	5V	5V	5V
1					1	0	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
1					1	0	0	1	0V*	0V*	0V*	0V*	0V*	0V*	0V*	0V*	0V*	0V*
1					1	0	1	0	12V	12V	12V	12V	12V	12V	12V	12V	12V	12V
1					1	0	1	1	5V	5V	5V	5V	5V	5V	5V	5V	5V	5V
1					1	1	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
1					1	1	0	1	0V*	0V*	0V*	0V*	0V*	0V*	0V*	0V*	0V*	0V*
1					1	1	1	0	12V	12V	12V	12V	12V	12V	12V	12V	12V	12V
1					1	1	1	1	3.3V	3.3V	3.3V	3.3V	3.3V	3.3V	3.3V	3.3V	3.3V	3.3V
1					1	1	1	1	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
1					1	1	1	0	0V*	0V*	0V*	0V*	0V*	0V*	0V*	0V*	0V*	0V*
1					1	1	1	1	12V†	12V†	12V†	12V†	12V†	12V†	12V†	12V†	12V†	12V†
1					1	1	1	0	0V*	0V*	0V*	0V*	0V*	0V*	0V*	0V*	0V*	0V*
1					1	1	1	1	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
1					1	1	1	1	0V*	0V*	0V*	0V*	0V*	0V*	0V*	0V*	0V*	0V*

X = don't care, \* clamped to ground, † illegal state per "The PC Card Specification."





# Functional Diagram



## Applications Information

PC Card power control for two sockets is easily accomplished using the MIC2564A PC Card/CardBus power controller. Control commands from a three-wire (plus Reset) serial bus determine  $V_{CC}$  and  $V_{PP}$  output voltages and select standby or operate mode.

$V_{CC}$  outputs of 3.3V and 5V at the maximum allowable PC Card current are supported. The  $V_{CC}$  outputs also support GND (0V) and high-impedance states. The  $V_{PP}$  outputs support  $V_{PP}$  (12V),  $V_{CC}$  voltages (3.3V or 5V), GND (0V), or high-impedance. When the  $V_{CC} = \text{Hi-Z}$  (high-impedance) condition is selected, the device switches into sleep mode and draws only leakage current.

Full protection during hot switching is provided which prevents feedback from the  $V_{CC}$  output (for example, from the 5V supply into the 3.3V supply) by locking out the low-voltage switch until the initial switch's gate voltage drops below 0.7V.

MIC2564A internal logic and MOSFET drive circuitry is powered from the  $V_{CC3}$  input and internal charge-pump voltage multipliers. Switching speeds are carefully controlled to prevent damage to sensitive loads and meet all PC Card specification timing requirements, including those for the CardBus option.

### Supply Bypassing

The MIC2564A is a switch and has no stability problems; however, supply bypass capacitors are recommended to reduce inductive transients and improve output ripple. As all internal device logic and comparison functions are powered from the  $V_{CC3}$  input, the power supply quality on this line is the most important. Micrel recommends placing 1 $\mu\text{F}$  surface-mount ceramic (low ESR) capacitors from  $V_{CC3}$  IN and  $V_{CC5}$  IN pins to ground and two 0.1 $\mu\text{F}$  surface-mount ceramic capacitors, one from each  $V_{PP}$  IN pin, to ground. Also, the  $V_{CC}$  OUT and  $V_{PP}$  OUT pins may use 0.01 $\mu\text{F}$  to 0.1 $\mu\text{F}$  capacitors for noise reduction and to reduce the chance of ESD (electrostatic discharge) damage.

### Power Status Feedback (Flags)

Two flag outputs monitor the  $V_{CC}$  and  $V_{PP}$  output voltages on both slot A and B, falling low when the voltage is not proper. Use of these open-drain flag outputs is optional; if they are used, a pull-up resistor to either the 3.3V or 5V supply is required. Unused flag outputs may be left open.

### PC Card Slot Implementation

The MIC2564A is designed for full compatibility with the PCMCIA (Personal Computer Memory Card International Association) PC Card Specification including the CardBus and Zoom Video (ZV) options.

When a PC card is initially inserted, it should receive  $V_{CC}$  (3.3V  $\pm$  0.3V or 5.0V  $\pm$  5%). The initial voltage is determined by a combination of mechanical socket keys and voltage sense pins. The card sends a handshaking data stream to the logic controller, which then determines if this card requires  $V_{PP}$  and if the card is designed for dual  $V_{CC}$ . If the card is

compatible with, and requires, a different  $V_{CC}$  level, the logic controller commands the power controller to make this change by disabling  $V_{CC}$ , waiting at least 100ms, and then re-enabling the other  $V_{CC}$  voltage.

If no card is inserted, or the system is in sleep mode, the logic controller commands the MIC2564A to shut down  $V_{CC}$ . This also places the switch into a shutdown (sleep) mode, where current consumption drops to nearly zero, with only tiny CMOS leakage currents flowing.

Internal device control logic, MOSFET drive and bias voltage is powered from  $V_{CC3}$  IN. The high voltage bias is generated by an internal charge pump multiplier. Input logic threshold voltages are compatible with common PC Card logic controllers using either 3.3V or 5V supplies.

### PC Card Voltage Regulation

The MIC2564A has been designed to meet or exceed PC Card voltage regulation specifications. The on-resistance of the FET switches will meet regulation requirements at 600mA and 1A respectively for  $V_{CC} = 5V \pm 3\%$  and 3.3V  $\pm 3\%$ .

### Flash Memory Implementation

When programming flash memory (standard +12V flash memories), the PC Card slot logic controller enables  $V_{PP}$  on the MIC2564A, which connects  $V_{PP}$  IN (nominally +12V) to  $V_{PP}$  OUT. The low on-resistance of the MIC2564A switch allows using a small bypass capacitor on the  $V_{PP}$  OUT pins, with the main filtering performed by a large filter capacitor on  $V_{PP}$  IN. (Usually the main power supply filter capacitor is sufficient.) Using a small-value capacitor such as 0.1 $\mu\text{F}$  on the output causes little or no timing delays.

The  $V_{PP}$  OUT transition from  $V_{CC}$  to 12.0V typically takes 200 $\mu\text{s}$ . After programming is completed, the logic controller signals to the MIC2564A, which then reduces  $V_{PP}$  OUT to the  $V_{CC}$  level. Break-before-make switching action and controlled rise times reduce switching transients and lower current spikes through the switch.

### Output Current and Protection

The MIC2564A meets or exceeds all PCMCIA specifications. MIC2564A output switches are capable of passing the maximum current needed by any PC Card. For system and card protection, output currents are internally limited. For full system protection, long term (longer than a few milliseconds) output short circuits invoke overtemperature shutdown, protecting the MIC2564A, the system power supplies, the card socket pins, board traces, and the PC Card. Individual internal status registers for each slot indicate when power problems exist.

### Control Bus Interface Overview

The MIC2564A power controller communicates with a logic controller (host adapter) via a 3-wire serial interface. A fourth control line attaches to the system reset line (RST#) and places all MIC2564A switches in the high-impedance (off) state. The reset function is active low.

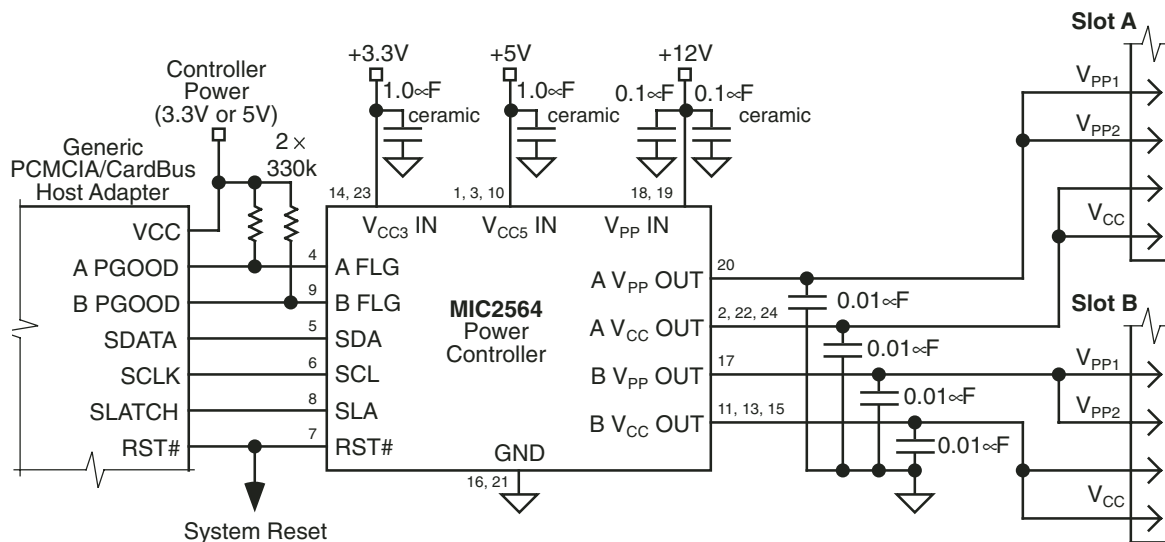


Figure 5. Generic "3-Wire" Serial Control Interface

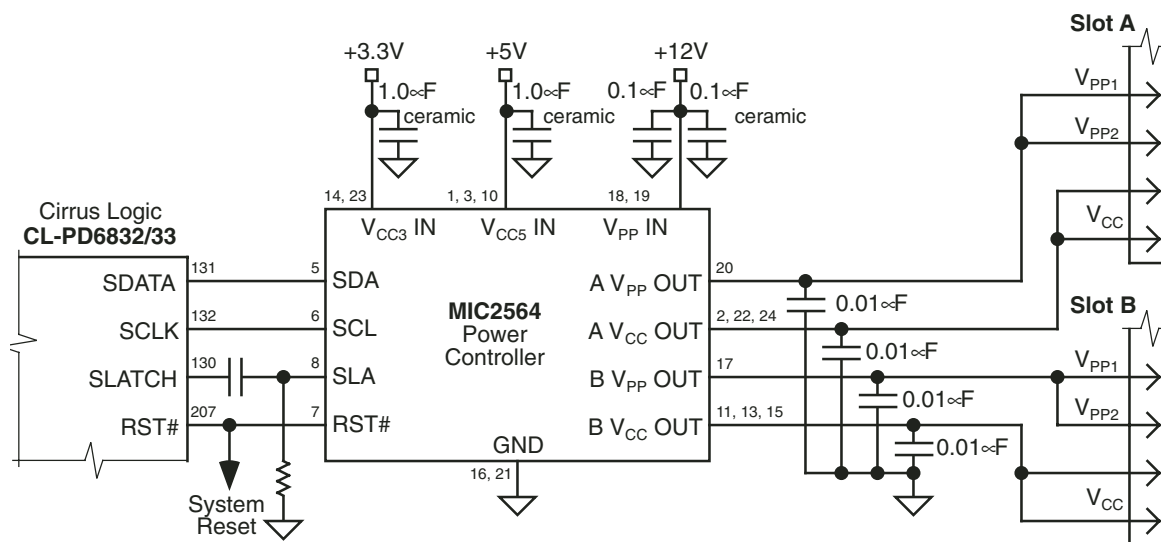


Figure 6. Cirrus Logic CL-PD6832 and CL-PD6833 Interface

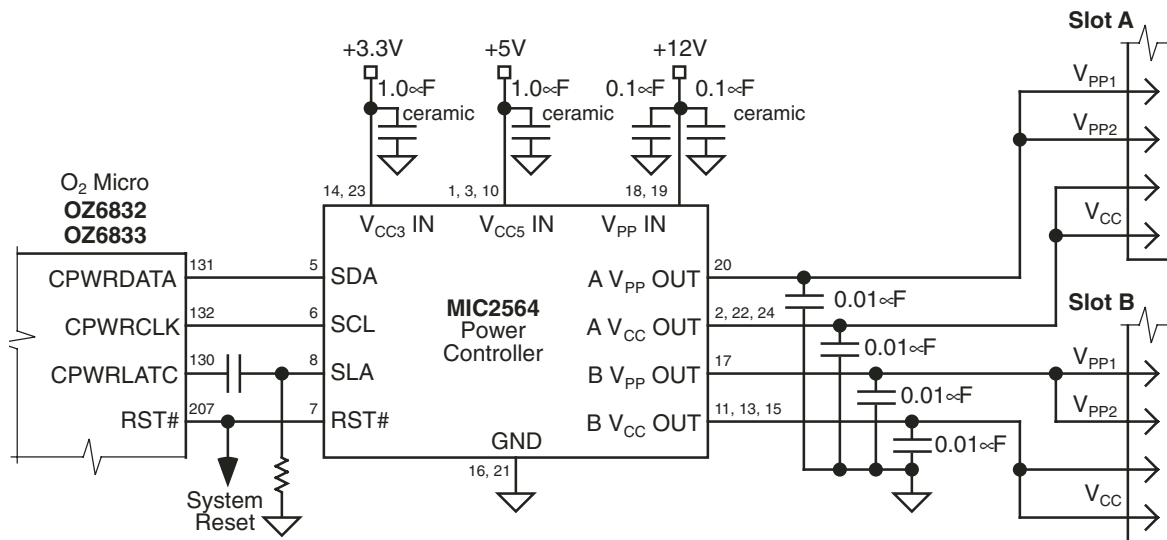


Figure 7. O<sub>2</sub> Micro OZ6833 and OZ6933

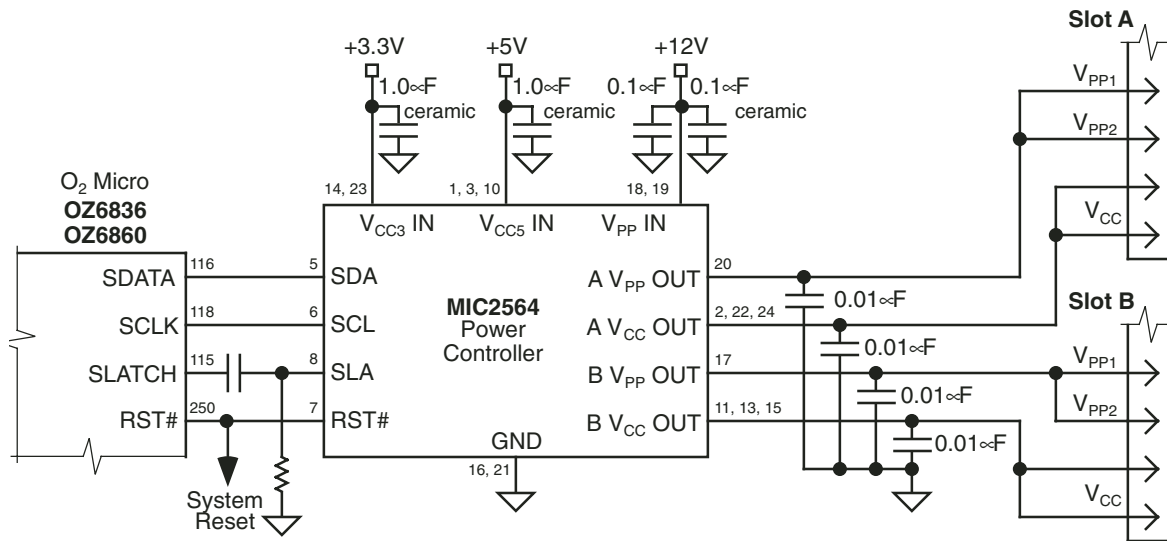
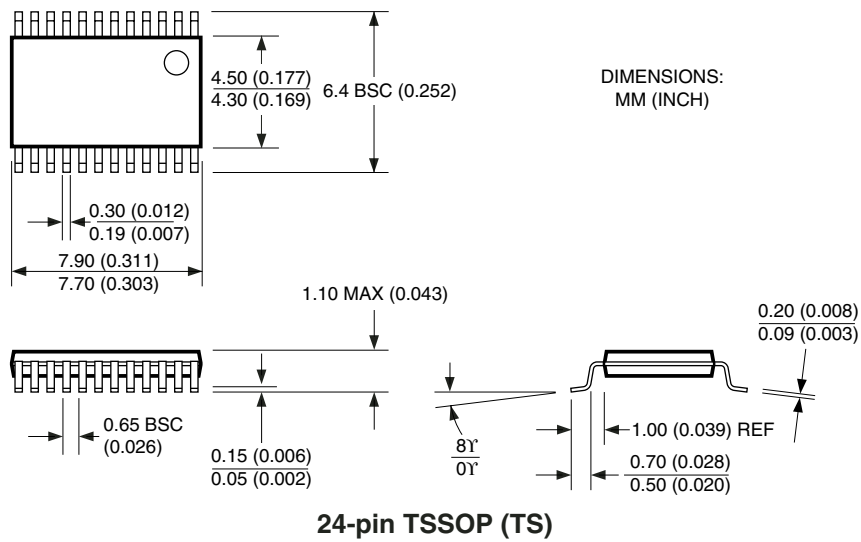
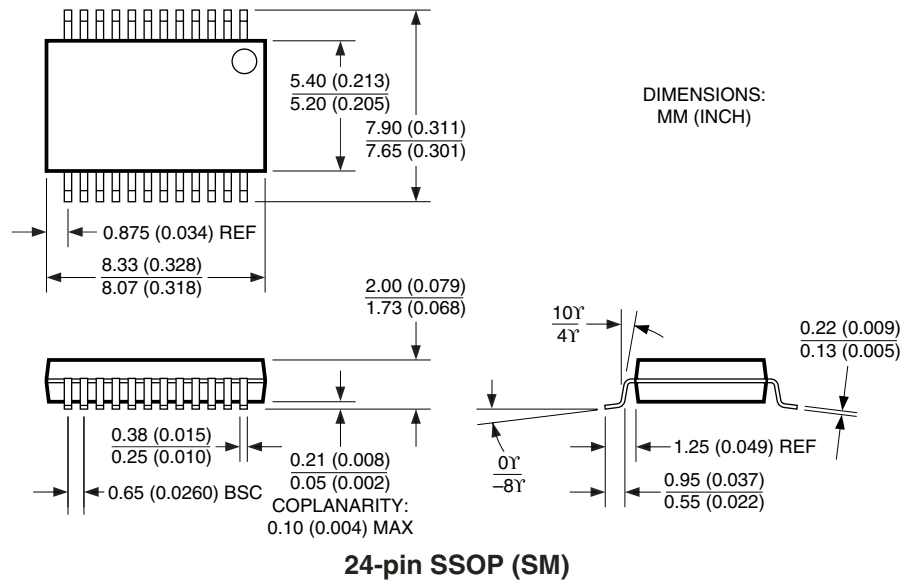


Figure 8. O<sub>2</sub> Micro OZ6860

# Package Information



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